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(54) Tuned switch-mode power supply with current mode control

(57) In a tuned switch mode power supply a zero voltage is maintained across a transistor switch (Q3), during both turn off and turn on switching transition intervals in the transistor switch. The tuned switch mode power supply operates in a current-mode control, on a current pulse-by-current pulse control basis. A modulator (31) of the power supply includes a pair of transistors (Q1, Q2) that form a regenerative switch to produce a portion of a control signal (VG) of the transistor switch that causes the transistor switch to turn off. A transformer-coupled input supply voltage (V1) maintains the transistor switch conductive as long as the current in the transistor switch does not exceed the threshold level of a regenerative switch. A resonant pulse (VD) is transformer-coupled from the resonant circuit to the regenerative switch for turning off the regenerative switch and for maintaining the transistor switch non conductive after the regenerative switch is turned off.

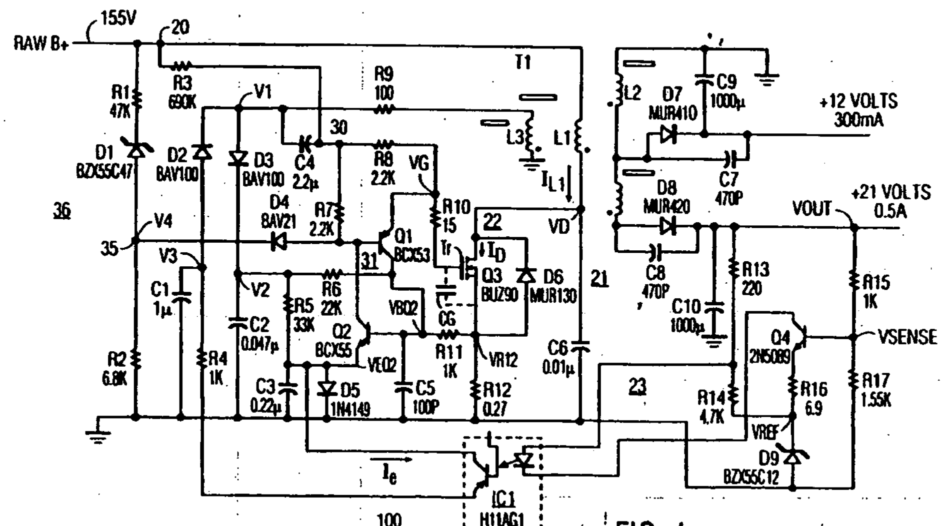

FIG. 1

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Description

The invention relates to a switch mode power supply.

A typical tuned switch-mode power supply (SMPS) includes a series arrangement of an inductance and a bi-directional controllable switch connected to input supply voltage terminals for receiving an input supply voltage. The switch is formed by a parallel arrangement of a transistor and a damper diode. A tuning capacitor is coupled to the inductance to form a resonant circuit. A drive or control circuit provides switching pulses for driving the switch alternately into the conducting and the cut-off states, the duration of the conducting state of the switch being controllable in dependence upon the output voltage by rectification of oscillations produced during periods when the switch is cut-off.

In such tuned SMPS, a substantially sinusoidal oscillation of a resonant pulse voltage of a large amplitude is developed in the inductance. The frequency of the oscillation is determined by the resonance frequency of the resonant circuit. After completion of a half cycle of oscillation the diode conducts and terminates the half cycle oscillation. The transistor is turned on when the diode is already conductive. Therefore, a zero voltage is maintained across the transistor, during the transition interval in the transistor. Thus, switching losses are reduced. In addition, the resonant circuit prevents the voltage that is developed across the transistor when the transistor is turned off from becoming excessive.

A modulator in a regulation control circuit of some prior art tuned SMPS's is responsive to an error signal produced in an error amplifier for varying a length of an interval when the bi-directional switch is conductive. The peak of the current in the inductance is thereby controlled. In this way, the amplitude of the resonant pulse voltage that is developed when the bi-directional switch is turned off is controlled for providing output voltage regulation.

Disadvantageously, in some prior art tuned SMPS's, variation of the input supply voltage is compensated in a relatively slow manner. The slow response time of the control circuit of such SMPS is determined mainly by the transient response of the feedback control loop. It may be desirable to speed up the response time of the tuned SMPS.

A tuned SMPS, embodying an inventive feature, operates in a current-mode control, on a current-pulse by current-pulse control basis. The current flowing in a switch terminates when it reaches a threshold level established by an error signal. The error signal actually controls the peak current in an inductance that is coupled to the switch. In this way, the control circuit corrects instantaneously in a feed forward manner for input voltage variations without using the dynamic range of the error amplifier. In this way, both the advantages of current mode regulation and of tuned SMPS are obtained.

A tuned switch mode power supply apparatus, embodying an aspect of the invention, includes a source of an input supply voltage and a tuned, resonant circuit. The resonant circuit includes a capacitance and an inductance coupled to the source of the input supply voltage. A first transistor switch is coupled to the inductance and is responsive to a periodic, switch control signal for generating current pulses in the inductance to produce resonant pulses in the resonant circuit. The resonant pulses are coupled to a load circuit for generating an output of the power supply. When the first transistor switch is being turned on, a substantially zero voltage is maintained between a pair of main current conducting terminals of the first transistor switch. A source of a second signal is used for controlling the output of the power supply in accordance with the second signal. A modulator is responsive to a given current pulse and to the second signal for generating the switch control signal. The power supply output is current mode controlled, in accordance with the second signal, on a current-pulse by current-pulse control basis.

In accordance with an inventive feature, the modulator includes a pair of transistors that form a regenerative switch to produce a portion of the control signal of the transistor switch that causes the transistor switch to turn off. The regenerative switch forms a latch that is triggered by a signal representative of the current pulse in the transistor switch. Advantageously, the transition of the control signal is speeded up by the positive feedback in the latch.

In accordance with another inventive feature, an error signal that is indicative of a difference between the output voltage of the power supply and a reference level is coupled to one of the pair of transistors to establish the triggering threshold level of the latch. In this way, advantageously, the one transistor of the pair also operates as a comparator.

In accordance with a further inventive feature, the inductance forms a first winding of a transformer for transformer-coupling the input supply voltage to a control terminal of the transistor switch when the transistor switch is conductive in a positive feedback manner. The transformer-coupled input supply voltage maintains the transistor switch conductive as long as the current in the transistor switch does not exceed the threshold level of the regenerative switch. The resonant pulse is transformer-coupled to the latch for turning off the regenerative switch. The resonant pulse is also transformer-coupled to the control terminal of the transistor switch in a positive feedback manner, and bypasses the regenerative switch, for maintaining the transistor switch non conductive after the regenerative switch is turned off.

FIGURE 1 illustrates a tuned SMPS embodying an aspect of the invention; and

FIGURES 2a, 2b and 2c illustrate wave forms useful for the explanation of the tuned SMPS of FIGURE 1.

FIGURE 1 illustrates a tuned SMPS 100, embodying an

aspect of the invention. In FIGURE 1, an N-type, metal oxide semiconductor (MOS) power transistor Tr operating as a transistor switch has a drain electrode coupled through a primary winding L1 of a transformer T1 to a terminal 20 of an input supply, direct current (DC) voltage B+. In a circuit configuration, not shown, the transformer can serve as an isolation transformer. Voltage B+ is derived from, for example, a filter capacitor coupled to a bridge rectifier that rectifies a mains supply voltage, not shown.

A source electrode of transistor Tr is coupled via a current sensor or sampling resistor R12. A damper diode D6 operating as a switch is coupled in parallel with transistor Tr and is included in the same package with transistor Tr to form a bi-directional switch 22. Capacitor C6 is coupled in parallel with diode D6 and in series with winding L1 to form with an inductance of winding L1 a resonant circuit 21 when switch 22 is non conductive.

A secondary winding L2 of transformer T1 is coupled to an anode of a peak rectifying diode D8 and to ground for generating an output voltage VOUT in a filter capacitor C10 that is coupled to a cathode of diode D8. Voltage VOUT is coupled to a load circuit, not shown. An error amplifier 23 includes a comparator transistor Q4 having a base electrode that is coupled to a voltage divider of voltage VOUT formed by resistors R15 and R17 where a voltage VSENSE is developed. Voltage VSENSE is equal to a corresponding portion of voltage VOUT and, thus, proportional to voltage VOUT.

An emitter electrode of transistor Q4 is coupled via a gain determining resistor R16 to a Zener diode D9 that develops a reference voltage VREF of error amplifier 23. Diode D9 is energized via series coupled resistors R13 and R14 from voltage VOUT. A photo-coupler IC1 includes a light emitting diode that is coupled between the collector of transistor Q4 and a junction terminal between resistors R13 and R14. An emitter electrode of the transistor of photo-coupler IC1 is coupled to a negative DC voltage V3 via a resistor R4. A collector electrode of the transistor of photo-coupler IC1 is coupled to capacitor C3. in a circuit configuration not shown the opto-coupler can serve for isolation. An error collector current Ie of the opto-coupler IC1 is indicative of an amount by which voltage VSENSE is greater than reference voltage VREF and, thus, of the difference there between.

A comparator transistor Q2 has a base electrode that is coupled via a resistor R11 to a junction terminal between the source electrode of transistor Tr and current sensor resistor R12. Transistor Q2 compares a base voltage VBQ2 of transistor Q2 to an error voltage VEQ2 developed at the emitter of transistor Q2. Voltage VBQ2 includes a first portion that is proportional to a source-drain current ID in transistor Tr. A DC voltage V2 is coupled via a resistor R6 to the base of transistor Q2 to develop a second portion of voltage VBQ2 across resistor R11.

DC voltage V2 is also coupled via a resistor R5 to a feedback loop filter formed by capacitor C3 to form a current source that charges capacitor C2. Error current Ie is coupled to capacitor C3 for discharging capacitor C3. A diode D5 is coupled between the emitter of transistor Q2 and ground. Diode D5 limits voltage VEQ2 to diode D5 forward voltage and limits the maximum current in transistor Tr.

The collector electrode of transistor Q2 is coupled to the base electrode of a transistor Q1 and the collector electrode of transistor Q1 is coupled to the base electrode of a transistor Q2 to form a regenerative switch 31. A control voltage VG of transistor Tr is developed at the emitter of transistor Q1 that forms an output terminal of regenerative switch 31 and is coupled to the gate electrode of transistor Tr via a resistor R10.

A secondary winding L3 of transformer T1 is coupled via a resistor R9 for producing an alternating current (AC) voltage V1. Voltage V1 is AC-coupled via a capacitor C4 and a resistor R8 to the emitter of transistor Q1 to generate drive voltage VG of transistor Tr. AC-coupled voltage V1 is coupled via a collector resistor R7 to the collector electrode of transistor Q2 and to the base electrode of transistor Q1. Voltage V1 is also rectified by a diode D2 to generate voltage V3 and by a diode D3 to generate voltage V2.

A resistor R3 coupled between the source of voltage B+ and a terminal 30 of capacitor C4 that is remote from winding L3 charges capacitor C4 upon power on or start up. When voltage VG on the gate electrode of transistor Tr exceeds a threshold voltage of MOS transistor Tr, Transistor Tr conducts causing a drain voltage VD of transistor Tr to decrease. As a result, voltage V1 becomes positive and reinforce voltage VG for maintaining transistor Tr, in a positive feedback manner, fully turned on.

FIGURES 2a-2c illustrate wave forms useful for explaining the operation of tuned SMPS 100 of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2c indicate similar items or functions.

During an interval t0-t1 of a given period T of FIGURE 2c, current ID of conductive transistor Tr of FIGURE 1 is up-ramping. Consequently, a corresponding non-resonant current pulse portion of a current IL1 in winding L1 is up-ramping and stores magnetic energy in the inductance associated with winding L1 of transformer T1. At time t1 of FIGURE 2c, voltage VBQ2 of FIGURE 1, containing an up-ramping portion derived from the voltage across resistor R12, exceeds a triggering level of regenerative switch 31 that is determined by voltage VEQ2 and turns on transistor Q2. Current flows in the base of transistor Q1 and regenerative switch 31 applies a low impedance at the gate electrode of transistor Tr. Consequently, gate electrode voltage VG of FIGURE 2a is reduced to near zero volts and turns off transistor Tr of FIGURE 1. When transistor Tr is turned off, drain voltage VD of FIGURE 2b increases and causes voltage V1 of FIGURE 1 that is coupled from winding L3 to decrease. The charge stored in gate-source capacitance CG maintains latch mode operation

until time t2 of FIGURE 2a.

In accordance with an inventive feature, when voltage VG becomes smaller than required to maintain sufficient collector current in transistor Q1 of FIGURE 1, a forward conduction on the base electrode of transistor Q2 ceases and, consequently, latch operation mode in regenerative switch 31 is disabled. Afterwards, voltage V1 that continues to decrease causes a negative portion 40 of voltage VG of FIGURE 2a to maintain transistor Tr of FIGURE 1 turned off.

When transistor Tr is turned off, drain voltage VD increases as shown during interval t1-t2 of FIGURE 2b. Capacitor C6 of FIGURE 1 limits the rate of increase of voltage VD such that transistor Tr is completely nonconductive before voltage VD increases appreciably above zero voltage. Thereby, switching losses and radiated switching noise are, advantageously, reduced.

Resonant circuit 21 that includes capacitor C6 and winding L1 oscillates, during interval t1-t3 of FIGURE 2b, when transistor Tr of FIGURE 1 is turned off. Capacitor C6 limits the peak level of voltage VD. Therefore, advantageously, no snubber diode and resistor are needed so that efficiency is improved and switching noise is reduced.

The decrease in voltage VD prior to time t3 of FIGURE 2b, causes voltage V1 of FIGURE 1 to become a positive voltage. At time t3 of FIGURE 2b, voltage VD is close to zero volts and slightly negative, causing damper diode D6 of FIGURE 1 to turn on and to clamp voltage VD of FIGURE 2b to approximately zero volts. Thus, resonant circuit 21 of FIGURE 1 exhibits a half cycle of oscillation. After time t3 of FIGURE 2b, voltage VG of FIGURE 2a becomes increasingly more positive, because of the aforementioned change in polarity of voltage V1 of FIGURE 1.

Advantageouly, the following turn on of transistor Tr is delayed by a delay time that is determined by the time constant of resistor R8 and gate capacitance CG until after time t3 of FIGURE 2b when voltage VD is nearly zero volts. Therefore, minimal turn-on losses are incurred and switching noise is reduced.

Negative feedback regulation of voltage VOUT is achieved by varying voltage VEQ2 in filter capacitor C3. When Voltage VSENSE that is proportional to voltage VOUT is larger than voltage VREF, current Ie discharges capacitor C3 and decreases voltage VEQ2. Therefore, the threshold level of comparator transistor Q2 is decreased. Consequently, the peak value of current ID in transistor Tr and the power delivered to the load circuit, not shown, are reduced. On the other hand, when voltage VSENSE is smaller than voltage VREF, current Ie is zero and the current in resistor R5 increases voltage VEQ2. Consequently, the peak value of current ID in transistor Tr and the power delivered to the load circuit, not shown, are increased.

In accordance with another inventive feature, tuned SMPS 100 operates in a current mode control, on a current-pulse by current-pulse control basis. The current pulse of current ID during interval t0-t1 of FIGURE 2c, flowing in transistor Tr of FIGURE 1, terminates at time t1 of FIGURE 2c when it reaches the threshold level of transistor Q2 of FIGURE 1 that is determined by voltage VEQ2 and is established by error current Ie forming an error signal. The error signal actually controls the peak current of the current pulse of current ID that flows in the inductance of winding L1. Advantageously, the control circuit corrects instantaneously in a feed forward manner for input voltage variations of voltage B+ without using the dynamic range of error amplifier 23. In this way, both the advantages of current mode regulation and of tuned SMPS are obtained.

As indicated before, DC voltage V2 is coupled via resistor R6 to the base of transistor Q2 to develop the second portion of voltage VBQ2 across resistor R11. During interval t0-t1 of FIGURE 2c, voltage V2 of FIGURE 1 is equal to voltage B+ multiplied by the turn ratio of windings L3 and L1 of transformer T1.

In accordance with a further inventive feature, the threshold level of transistor Q2 varies in accordance with voltage V2 and, therefore, in accordance with voltage B+. Thus, the peak value of current ID also varies in accordance with voltage B+. Advantageously, this feature tends to maintain a constant power delivery capability of SMPS 100 so that excessive power cannot be delivered at high AC mains supply voltage, not shown.

In accordance with an additional inventive feature, startup at abnormally low input voltage B+ is inhibited by a diode D4 having an anode that is coupled to the base of transistor Q1 and a cathode that is coupled to a junction terminal 35 of a voltage divider 36. Voltage divider 36 is coupled between voltage B+ and ground and include the series arrangement of a resistor R1, a Zener diode D1 and a resistor R2 such that terminal 35 is coupled between Zener diode D1 and resistor R2. At low input voltage B+, Zener diode D1 is turned off and a voltage V4 at terminal 35 causes diode D4 to conduct in a manner to turn on transistor Q1 and disable transistor Tr. On the other hand, at normal levels of voltage B+, diode D1 is conductive and diode D4 is back biased and has no effect on circuit operation.

Claims

1. A tuned switch mode power supply apparatus, comprising:

   a source of an input supply voltage (RAW B+);
   a tuned, resonant circuit including a capacitance (C6) and an inductance (L1) coupled to said source of said input supply voltage;
   a first transistor switch (Q3) coupled to said inductance and responsive to a periodic, switch control signal (V6) for generating current pulses in said inductance to produce resonant pulses (VD) in said resonant circuit that are coupled to a load circuit for generating an output (VOUT) of said power supply such that, when said first transistor switch is being turned

on, a substantially zero voltage is maintained between a pair of main current conducting terminals (COLLECTOR-EMITTER) of said first transistor switch;

a source of a second signal (VEQ2) for controlling said output of said power supply in accordance with said second signal; and characterized by

a modulator (31, R12) responsive to a given current pulse (I_{L1}) and to said second signal for generating said switch control signal such that said power supply output is current mode controlled, in accordance with said second signal, on a current-pulse by current- pulse control basis.

2. An apparatus according to Claim 1 characterized in that in a given switching period of said first transistor switch (Q3), said resonant pulse (VD) forms one half cycle of oscillation in said resonant circuit (21).

3. An apparatus according to Claim 1 further characterized by, a second switch (D6) coupled to said transistor switch (Q3) for applying a low impedance between said main current conducting terminals to maintain the substantially zero voltage between said main current conducting terminals of said first transistor switch when said first transistor switch is being turned on.

4. An apparatus according to Claim 3 characterized in that said second switch (D6) comprises a damper diode that is coupled in parallel with said first transistor switch (Q3).

5. An apparatus according to Claim 1 further characterized by, a resistor (R12) coupled in series with said first transistor switch for generating a ramping voltage (VR12) that is indicative of a ramping portion of said current pulse such that said switch control signal (V6) causes the state of said first transistor switch to change, during said ramping portion of said given current pulse, when said given current pulse exceeds a level that is determined by said second signal (VEQ2).

6. An apparatus according to Claim 1 characterized in that a change in said second signal (VEQ2) affects substantially more a length of an interval between adjacent resonant pulses and substantially less a pulse width of said resonant pulse.

7. An apparatus according to Claim 1 characterized in that said modulator (31, R12) comprises a comparator, second transistor (Q2) having a control terminal (BASE) responsive to said current pulse, a first main current conducting terminal (EMITTER) responsive to said output (VOUT) of said power supply and a second main current conducting terminal (COLLECTOR) coupled to a third transistor (Q1) in a positive feedback manner to form therewith a regenerative switch (31) that is coupled to a control terminal (BASE) of said first transistor switch (Q3).

8. An apparatus according to Claim 7 characterized in that said current pulse (I_{L1}) varies in a ramping manner and produces a switching transition in said regenerative switch (31) when said current pulse exceeds a threshold level that is determined by said second signal (VEQ2) to operate said regenerative switch in a latch mode of operation, and wherein said resonant pulse (VD) is coupled to said regenerative switch for producing an opposite change of state in said regenerative switch.

9. An apparatus according to Claim 8 characterized in that said resonant pulse (VD) is coupled to said regenerative switch to disable the latch operation.

10. An apparatus according to Claim 1 characterized in that said source of said second signal (VEQ2) comprises a comparator (Q4) responsive to said output (VOUT) of said power supply and to a signal at a reference level (VREF) for generating an error signal (I_e) that is coupled to said modulator (31, R12) via a feedback loop filter (C3) to develop said second signal at an output of said filter.

11. An apparatus according to Claim 1 characterized in that a capacitance (C6) that is coupled to one of said main current conducting terminals (COLLECTOR) of said first transistor switch (Q3) substantially reduces a rate of change of said voltage (COLLECTOR-EMITTER) between said pair of main current conducting terminals when said first transistor switch is being turned off.

12. An apparatus according to Claim 1 further characterized by, a regenerative switch (31) responsive to said current pulse (I_{L1}) and coupled to a control terminal (BASE) of said first transistor switch (Q3) wherein when said current pulse exceeds a threshold level (VEQ2) of said regenerative switch, said regenerative switch, operating as a latch, is triggered, and wherein said resonant pulse (VD) is coupled to said regenerative switch (via R9) for disabling the latch operation in said regenerative switch and is also coupled to said control terminal (BASE) of said first transistor switch in a manner that bypasses said regenerative switch (via R10) for maintaining said first transistor switch nonconductive following a time when the latch operation is disabled.

13. An apparatus according to Claim 12 characterized in that said resonant pulse (VD) maintains said first transistor switch (Q3) nonconductive as long as a

magnitude of said resonant pulse is within a range of values, and produces a switching transition when said magnitude of said resonant pulse is outside said range of values (>RAW B+).

14. An apparatus according to Claim 1 further characterized by, a first winding (L3) of a transformer having a second winding (L1) that is coupled to one of said main current conducting terminals (COLLECTOR) of said first transistor switch (Q3) and to said source of input supply voltage (RAW B+) for transformer-coupling said input supply voltage to a control terminal (BASE) of said first transistor switch via said first winding in a positive feedback manner to produce said control signal (VG) at a first state (HIGH), during a first portion of a period, wherein said resonant pulse is coupled to said control terminal of said first transistor switch via said first winding in a positive feedback manner for producing said control signal at a second state (LOW), during a second portion of said period.

15. An apparatus according to Claim 14 further characterized by, a regenerative switch (31) responsive to said current pulse (I_{L1}) and coupled to a control terminal (BASE) of said first transistor switch (Q3) wherein, during said first portion of said period, when said current pulse exceeds a threshold level of said regenerative switch, said regenerative switch operates as a latch that is triggered in a first direction (TURNED ON) and wherein said resonant pulse (VD) is coupled to said regenerative switch for disabling the latch operation and is also coupled to said control terminal for maintaining said switch nonconductive following a time when the latch operation is disabled.

16. A switch mode power supply apparatus, comprising:

a source of an input supply voltage (RAW B+);
a resonant circuit (21) including a capacitance (C6) and an inductance (L1) coupled to said source of said input supply voltage;
a first transistor switch (Q3) coupled to said inductance and responsive to a periodic, switch control signal (VG) for generating current pulses in said inductance (I_{L1}) to produce resonant pulses in said resonant circuit that are coupled to a load circuit for generating an output (VOUT) of said power supply;
a second switch (D6) coupled to said transistor switch for maintaining a substantially zero voltage between a pair of main current conducting terminals (COLLECTOR-EMITTER) of said first transistor switch, during a switching transition interval, when said first transistor switch is being turned on;
a source of a second signal (VEQ2) for controlling a magnitude of said output of said power supply in accordance with said second signal; and characterized by
a regenerative switch (31) responsive to a periodic, third signal (VBQ2) and to said second signal and coupled to a control terminal of said first transistor switch (BASE), said regenerative switch operating as a latch that is triggered when a first difference between said third and second signals occurs, said regenerative switch being responsive to said resonant pulse for disabling the latch operation when said resonant pulse is generated, such that after the latch operation is disabled, said resonant pulse is coupled to said control terminal for maintaining a state (NON-CONDUCTION) of said first transistor switch unchanged.

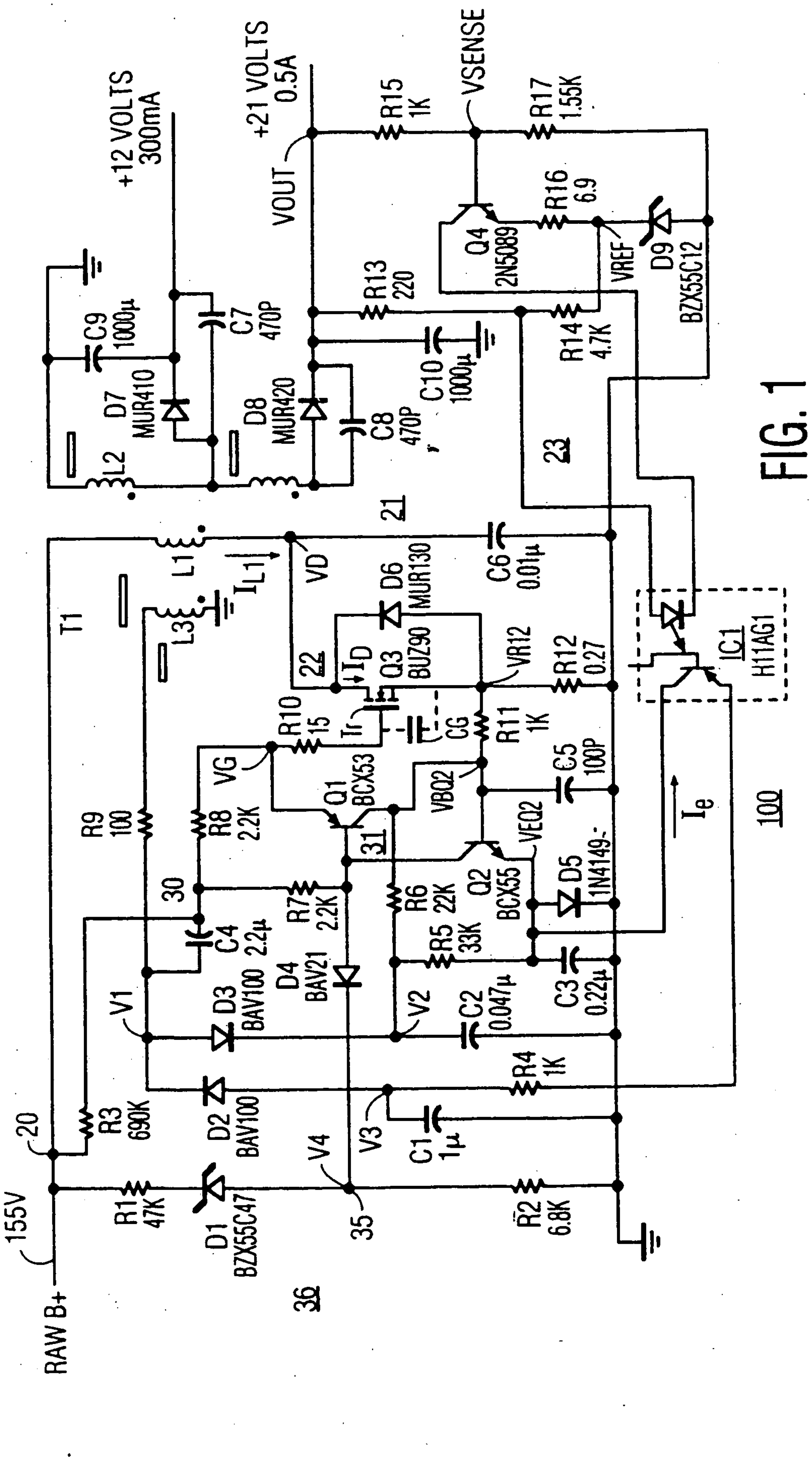
17. An apparatus according to Claim 16 further characterized by, a first winding (L3) of a transformer for transformer-coupling said input supply voltage to said control terminal (BASE) of said first transistor switch via said first winding to produce a change of state (TURN ON) in said control signal (V6) following a portion of said resonant pulse.

18. A switch mode power supply apparatus, comprising:

a source of an input supply voltage (RAW B+);
a resonant circuit (21) including a capacitance (C6) and an inductance (L1) coupled to said source of said input supply voltage;
a transistor switch (Q3) coupled to said inductance and responsive to a periodic, switch control signal (VG) for generating current pulses in said inductance (I_{L1}) to produce resonant pulses (VD) in said resonant circuit that are coupled to a load circuit for generating an output (VOUT) of said power supply;
a damper diode (D6) coupled to said transistor and responsive to said resonant pulse for maintaining a substantially zero voltage between a pair of main current conducting terminals of said transistor switch (COLLECTOR-EMITTER), when said transistor is being turned on;
a source of a second signal (VEQ2) for controlling said output of said power supply in accordance with variations of said second signal; and characterized by
a comparator, second transistor (Q2) responsive to a periodic, third signal (VBQ2) and to said second signal and coupled to a third transistor (Q1) to form therewith a regenerative switch (31) that is coupled to a control terminal (BASE) of said first transistor switch to generate said control signal, said regenerative switch operating as a latch that is triggered in a first direction when a first difference between said

periodic, third signal and said second signal occurs, said latch being responsive to said resonant pulse for disabling the latch operation when said resonant pulse is generated.

19. An apparatus according to Claim 18 further characterized by a first winding (L3) of a transformer for transformer-coupling said input supply voltage (RAW B+) to said control terminal (BASE) of said transistor switch to maintain said transistor switch (Q3) at a first state (CONDUCTIVE) before said latch is triggered and for transformer-coupling said resonant pulse (VD) to said control terminal to maintain said transistor switch at a second state (NON-CONDUCTIVE) after said latch is disabled.


+12 VOLTS
300mA
+21 VOLTS
0.5A
VOUT
VSENSE
R15
1K
R17
1.55K
R16
6.9
Q4
2N5089
VREF
D9
BZX55C12
R13
220
R14
4.7K
C9
1000μ
C7
470P
D7
MUR410
L2
D8
MUR420
C8
470P
C10
1000μ
23
21
T1
L1
I_{L1}
VD
C6
0.01μ
L3
D6
MUR130
22
I_D
Q3
BUZ90
VR12
R12
0.27
IC1
H11AG1
R10
15
Tr
CG
R11
1K
VG
R9
100
R8
2.2K
Q1
BCX53
VBQ2
C5
100P
I_e
100
30
31
R7
2.2K
R6
22K
Q2
BCX55
VEQ2
D5
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C4
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R5
33K
C3
0.22μ
D3
BAV100
D4
BAV21
V1
V2
C2
0.047μ
R4
1K
R3
690K
D2
BAV100
V3
C1
1μ
20
V4
155V
R1
47K
D1
BZX55C47
35
R2
6.8K
36
RAW B+

FIG. 1

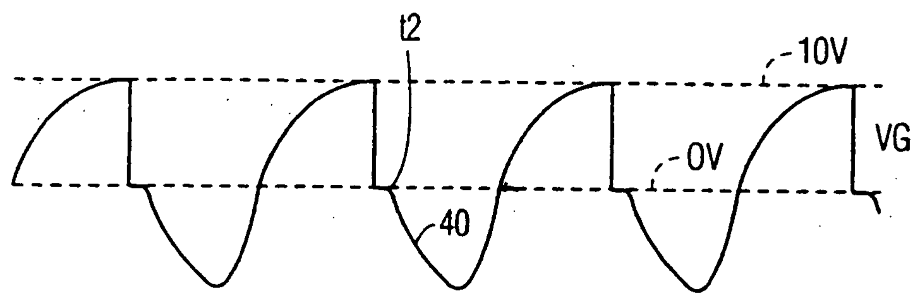

FIG. 2a

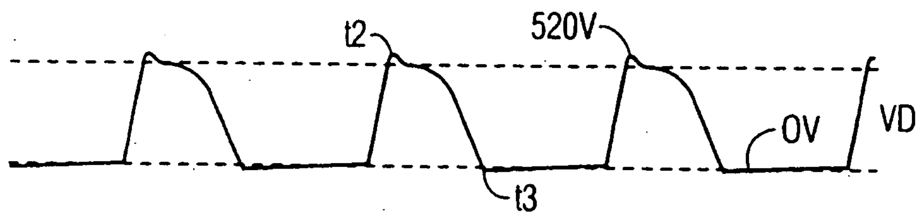

FIG. 2b

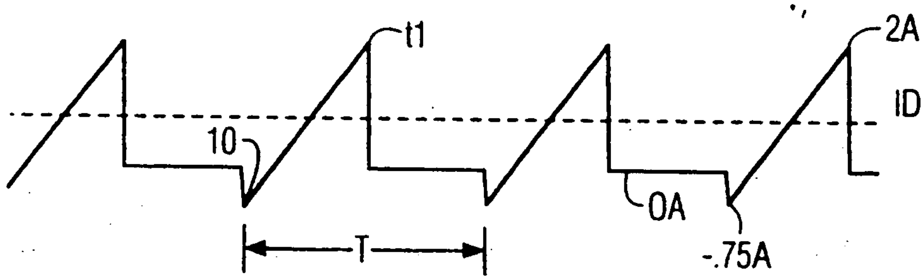

FIG. 2c

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(54) **Tuned switch-mode power supply with current mode control**

(57) In a tuned switch mode power supply a zero voltage is maintained across a transistor switch (Q3), during both turn off and turn on switching transition intervals in the transistor switch. The tuned switch mode power supply operates in a current-mode control, on a current pulse-by-current pulse control basis. A modulator (31) of the power supply includes a pair of transistors (Q1, Q2) that form a regenerative switch to produce a portion of a control signal (VG) of the transistor switch that causes the transistor switch to turn off. A transformer-coupled input supply voltage (V1) maintains the transistor switch conductive as long as the current in the transistor switch does not exceed the threshold level of a regenerative switch. A resonant pulse (VD) is transformer-coupled from the resonant circuit to the regenerative switch for turning off the regenerative switch and for maintaining the transistor switch non conductive after the regenerative switch is turned off.

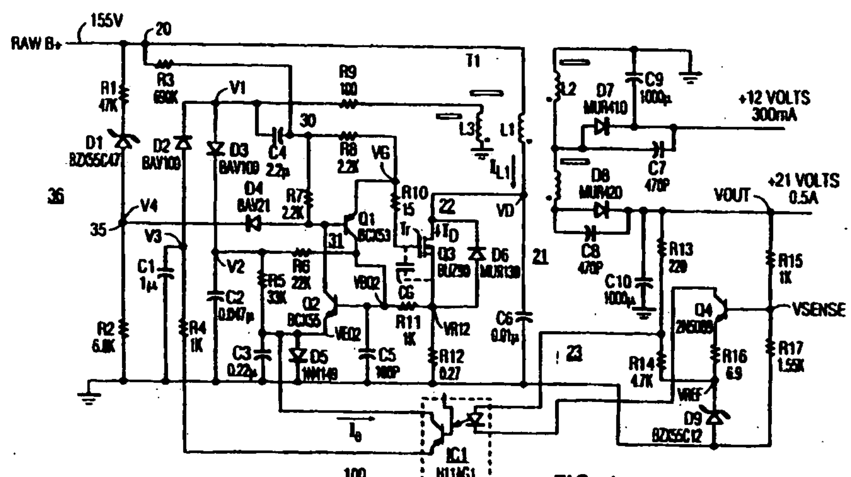

FIG. 1

EP 0 767 528 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 96 11 5765

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 086 521 A (PHILIPS NV) 24 August 1983 * page 3, line 13 - page 7, line 13; figure *	1,2,5,6	H02M3/335 H02M3/338
A		7-10, 12-19	
A	US 5 171 949 A (FUJISHIMA KUNIHIRO ET AL) 15 December 1992 * column 2, line 34 - column 3, line 66; figures 1-4 *	3,4,16, 18	
A	EP 0 049 633 A (TEXAS INSTRUMENTS INC ;TEXAS INSTRUMENTS LTD (GB)) 14 April 1982 * page 6, line 15 - page 15, line 18; figures 1-7 *	1,2,5-8, 10,11, 16,18	
A	EP 0 091 133 A (SANYO ELECTRIC CO) 12 October 1983		
A	FR 2 575 617 A (STANLEY ELECTRIC CO LTD) 4 July 1986		TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	US 4 903 182 A (PILUKAITIS RAYMOND W ET AL) 20 February 1990		H02M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 May 1998	Albertsson, E

CATEGORY OF CITED DOCUMENTS

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